Claims

1.-16. (canceled)

17. (previously presented) A method for testing an integrated circuit having multiple analog nodes and testing circuitry, comprising:

selecting an analog node in the integrated circuit from a list of analog nodes stored in a memory;

obtaining a test value from the selected analog node;

retrieving a tolerance value associated with the selected analog node from a memory; and

comparing the test value of the selected analog node with the tolerance value, wherein the comparing is performed by a condition checker in the testing circuitry, the condition checker performing comparisons of test values and tolerance values for plural analog nodes in the integrated circuit.

18. (original) The method of claim 17 wherein the associated tolerance value is retrieved from the same memory in which the list of analog nodes is stored.

19. (original) The method of claim 17, wherein the comparing comprises checking whether the test value of the selected analog node is within the associated tolerance value.

20. (original) The method of claim 19 further comprising generating an error indication signal in response to the checking.

21. (original) The method of claim 20 further comprising:

reconfiguring a memory in the integrated circuit to be operable to store diagnostic data from the testing circuitry.

22. (original) The method of claim 21 further comprising:

storing data identifying the selected analog node in the memory; and

storing the test value of the selected analog circuit in the memory.

23. (previously presented) The method of claim 20 further comprising:

storing data identifying the selected analog node in a data memory in the testing circuitry; and

storing the test value of the selected analog node in a data memory in the testing circuitry.

24. (original) The method of claim 23 wherein the data identifying the selected analog node and the test value of the selected analog circuit are stored in the same data memory.

25. (original) The method of claim 24 further comprising:

obtaining a test value of a second analog node, wherein the second analog node is associated with the selected analog node;

storing data identifying the second analog node in the data memory; and

storing the test value of the second analog node in the data memory.

26. (original) The method of claim 24 further comprising uploading the contents of the data memory to a host computer.

27. (original) The method of claim 17 wherein the obtaining is responsive to stimuli transmitted to the integrated circuit from a location outside the integrated circuit.

28. (original) The method of claim 17 further comprising:

prior to the comparing, selecting a condition checker in the testing circuitry for performing the comparing.

29. (original) The method of claim 17 further comprising, prior to the selecting:

storing data identifying the analog nodes of the integrated circuit in a program memory in the testing circuitry;

storing tolerance values associated with the analog nodes of the integrated circuit in the program memory.

30.-36. (canceled)